ParBERT 81250 Changes and Enhancement History

Date	Revision	Reason
13.06.2000	**1.0**	**Initial release**
03.07.2000	1.01	
11.07.2000	1.02	
04.08.2000	1.03	
08.08.2000	1.04	
11.08.2000	1.05	
02.08.2000	1.07	
14.08.2000	1.08	
16.08.2000	**1.1**	**Major enhancement**
17.08.2000	1.11	
06.09.2000	1.12	
12.10.2000	1.13	
10.01.2001	1.14	
31.01.2001	1.15	
19.02.2001	1.16	
29.03.2001	**3.0**	**Major enhancement**
09.04.2001	3.01	
03.05.2001	3.01 SP1	
20.07.2001	3.50	
25.07.2001	3.51	
30.07.2001	**3.52**	**Major enhancement**
22.08.2001	3.52_SP1	
26.10.2001	3.52_SP2	
05.10.2001	3.90	
12.10.2001	3.91	
09.11.2001	**4.00**	**Major enhancement**
30.11.2001	**4.10**	**Major enhancement**
05.12.2001	4.11	
13.12.2001	4.12	
09.01.2002	4.12 SP1	
12.02.2002	**4.20**	**Major enhancement**
20.12.2002	4.20 SP1	
20.02.2002	4.20 SP2	
12.03.2002	4.20 SP3	
18.04.2002	**4.30**	**Major enhancement**
30.04.2002	4.30 SP1	
10.06.2002	4.30 SP2	
11.07.2002	**4.5**	**Major enhancement**
19.07.2002	4.50 SP1	
29.07.2002	4.50 SP2	
14.10.2002	4.50 SP3	
03.12.2002	**5.0**	**Major enhancement**
09.12.2002	5.0 SP1	
24.02.2003	**5.1**	**Major enhancement**
18.03.2003	5.11	
28.05.2003	**5.20**	**Major enhancement**
23.06.2003	5.20 SP1	
09.10.2003	5.20 SP2	
09.12.2003	**5.50**	**Major enhancement**
18.12.2003	5.50 SP1	
13.01.2004	5.50 SP2	
23.01.2004	5.50 SP3	
23.01.2004	5.50 SP4	
10.03.2004	5.51	
19.03.2004	5.52	
14.04.2004	5.53	
16.04.2004	**5.60**	**Major enhancement**
23.04.2004	5.61	
21.05.2004	5.62	
14.06.2004	5.63	
16.06.2004	5.64	
06.07.2004	5.65	
13.09.2004	5.66	
27.09.2004	5.67	
16.11.2004	5.68	
13.12.2004	5.69	

Known Problems

- **Waveform-Viewer**: analyzer signal not shown with low frequency (e.g. 1KHz). This might not be a problem for ParBERT; here we always have frequencies above 330KHz!
- **Waveform-Viewer**: wrong marker range. E.g. range 0..798ns marker vernier 0..798, markers slider 0…799
- **Waveform-Viewer**: markers sometimes not visible. E.g. range 0..798ns, window 745...753ns, 1ns/div., marker position A+B 746ns invisible.
- **Waveform-Viewer**: marker placement. Marker A set to 1 ns, Marker B set to 0 ns using the vernier. A to B = 0 displayed, both Markers are positioned at the same place.
- **Waveform-Viewer**: Transition on last Pattern from 0 to 1, sometimes this transitions is visible, sometimes it remains 0 depending on time slider position.
- **Waveform-Viewer / Segment Editor interoperation**: Waveform-Viewer keeps segments open. This results in the strange effect that if you make changes to a segment in the segment editor and want to cancel these changes by closing the segment editor and saying no to "Do you want to save your changes?" the changes actually remain in the buffer until the waveform-viewer is closed. Reopening the segment editor on that segment before closing the waveform-viewer still shows all the changes. Note that the changes are actually not on disk, just in a buffer so when all viewers of that segment are closed the changes are actually thrown away as desired.
- **Waveform-Viewer** display refresh problem: When moving marker A around sometimes the hex-values of bus-signals are redraw n at other locations
- **Waveform-Viewer**: after port delete sometimes forgets its signals. Example: have two ports, waveform-viewer open. Delete first port -> the signals in the waveform-viewer vanish... Delete second port -> just the signals of the no longer available port vanish.
- **Waveform-Viewer**: empty waveform viewer with segment resolution 16 and 2ns/div
- External Reference Mode does not allow Data frequencies below the external reference clock frequency. E.g. for external reference 10MHz it is not possible to have user frequency below 10MHz. The same is true for 5, 2, 1MHz. shouldn't we add this to the specs and don't show it as a known bug?
- **File Browser - Details**: Multiple instead of single selection
- Sequence expressions that are syntactically incorrect might crash the GUI. Can only happen in combination with an incorrect remote program.
- **E4808A**: PLL does not lock. Very early shipped E4808A Versions have a hardware bug: When using the external clock divider other than 1, the PLL shows unlock. If this problem is seen the module must be sent in for repair.
- **E4808A** in Master Slave Configuration shows self-test error "Sysclk Cable cross wired". This is caused by a hardware bug in earlier shipped E4808A modules (before serial number DE41900158). If this problem is encountered the module must be sent in for repair.
- Right clicks sometimes immediately execute whatever lies behind the mouse pointer when the pop-up menu appears. This will always happen if the pop-up menu does not fit on the screen without being moved. Moving the GUI on the screen to a position that guarantees a 'complete' pop-up menu will give normal behavior.
- The Standard Mode Sequence Editor does not support Fast Bit Synchronization.
- The first trigger pulse on the E4809A is intermittent delayed by some picoseconds.
- The module E4861A fails intermittent to synchronize on ERRORED-PRBS pattern depending on delay settings.
- Installation under very rare circumstances installs the Software in the Windows System directory. Everything works fine, but uninstalling is not possible. As workaround remove all files manually and delete environment variable DVTDSRBASEDIR.

Graphical User Interface or Firmware Server doesn't respond

In case the Graphical User Interface or the Firmware Server doesn't respond in a system with multiple GUI's and Firewire connection you should upgrade to the newest I/O Library for Instrument Control.
At least Revision J.02.00.01 or later is recommended. You can download the latest released version of the Agilent IO Libraries from http://www.agilent.com/find/iolib

GPIB - Gateway problem

The way the GPIB card is operated as non-controller (to provide the interface of an instrument) has been improved. Unfortunately, if a system is opened for access for the first time it can happen that an erroneous answer is transmitted via GPIB bus and the communication is blocked afterwards. A workaround for this behavior was opening all systems to be used in GUI sessions - which sometimes is not applicable in production environments. To FIX this behavior, the user should do the following:

For opening a system handle, always use the OpenHandleEx() function code which handles the erroneous answer and the timeouts properly (C/C++ sample follows).

```
// sample code for safely opening a system handle via VISA
ViStatus OpenHandleEx(ViSession vi, char *SystemName, char *HandleTemplate, char
*Answer)
{
        ViStatus status;
        status= viQueryf( vi, ":DVT:INST:HAND:CRE? %s,\"DSR\",\"%s\"\n", "%t",
        HandleTemplate, SystemName, &Answer );
        if( status < VI_SUCCESS )
        {
                int i = 90;
                // in a loop, we try to read the answer for the request, if we had no
                // success in the viQueryf call (i.e. it timed out)
                while ((i > 0) && (status < VI_SUCCESS))
        {
        Sleep(50); // a little delay time where we don't touch the Interface
        status=  viScanf(vi,"%t", &Answer);
        i--;
        }
        if( status >= VI_SUCCESS )
        {
                // Now we have at least a result for the request. But due to the possible
                // interface reset, it can be a nonsens string. Because of that we do a
                // plausibility check here to get sure we have the right handle.
                 // If we suppose we didn't receive the right answer, we try to get it by
                 // issuing a useless request.
                // normally, the Firmware prepends an underscore to the template name
                // upon success, so SYSTA becomes _SYSTA or _SYSTAA
                if( strncmp(&Answer[1], HandleTemplate, strlen(HandleTemplate)) != 0 )
        {
        // handle did not contain the Template - must be wrong, we have
        // to do a re-read attempt, for safety we ask for the handle again
        status=  viQueryf(vi, ":DVT:INST:HAND:CRE? %s,\"DSR\",\"%s\"\n", "%t",
        HandleTemplate, SystemName, &Answer);
        while ((i > 0) && (status < VI_SUCCESS))
                {
                Sleep(50); // a little delay time where we don't touch the IF lines
                status =  viScanf(vi,"%t", &Answer);
                i--;
        }
        }
        }
        }
        return status;
}

// Main program
        #define HDL_LEN         64

ViSession Ag81250;              // Virtual instrument handle (Agilent 81250)
ViSession DRM;                          // Default Resource Manager
ViStatus status;                // Return status
```

```
char hdl [HDL_LEN]= {0};

        // This function returns a session to the Default Resource Manager
        // resource.
        status= viOpenDefaultRM(&DRM);
        ...
        // This function opens a session to the Agilent 81250 at GPIB address 11.
        // It returns a session identifier that can be used to call any other
        // functions to Agilent 81250.
        status= viOpen(DRM, "GPIB0::11::INSTR", VI_NULL, VI_NULL, &Ag81250);
        ...
        // Open a connection to the "DSRA" 81250 system
        status= OpenHandleEx(Ag81250, "DSRA", "SYSTA", hdl);
        ...
        // Now if the request returned VI_SUCCESS, hdl contains the handle
        // and can be used to program the 81250 system
        status= viPrintf(Ag81250, ":%s:SGEN:GLOB:PER  2.5e-9\n", hdl);
        ...
```

Bug fixes for 5.69 release

- Full support for WindowsXP
- File Browser - Details: Multiple instead of single selection
- GUI dies on XP OS, when screensaver is invoked
- Installation issues resolved

List of known problems for 5.69 release

- Segment Editor: data window jumps back to offset 0
- Right Click shows undefined behavior
- SMSE chooses invalid block length for fast bit sync
- Installation / Deinstallation does not work any more
- XGbE Tool: CJ- and CR-Pattern on real XAUI DUT does not work
- System User Guide - Deskewing: wrong connector types of 13.5G
- Description of the Deskewing process for E4809A is incomplete.
- Setting the Delay System before establishing connection fails
- MUI: Eye Opening: ISO-BER interpolation wrong!
- If MUI not visible no Status events started in sync mode
- MUI always loads setting when opening a workspace or measurement
- Wrong B-1 value of concatenated scrambled multiple frames (SONET-C)
- Output Levels MUI - decimal precision of BER axis not modifiable
- Eye opening MUI - decimal precision of BER Threshold not modify
- Cable deskew not working unless common mode voltage is zeroed.
- MUI Output Timing strange Jitter Values
- Wrong tab-order in MUI Spectral Jitter / Properties

Bug fixes for 5.68 release

- N4873A speed improvement on connect and disconnect
- N4872A, N4873A speed improvement on frequency change (only inside the same range)
- Measurements are in an infinite loop, when fast bit sync is used
- E4808A, E4809A: power supply self-test uses too tight limits
- Delay slider missing, in GUI, for 3.3G modules

List of known problems for 5.68 release

- See 5.63 release

Bug fixes for 5.67 release

- Added delay slider for N4872A, E4862B and E4810A

List of known problems for 5.67 release

- See 5.63 release

Bug fixes for 5.66 release

- Improvements in the MUI:
  - MUI always loads setting when opening a workspace or measurement
  - Output Levels MUI - decimal precision of BER axis not modifiable
  - Eye opening MUI - decimal precision of BER Threshold not modify
  - MUI Output Timing strange Jitter Values
  - Wrong tab-order in MUI Spectral Jitter / Properties
- N4873A: GUI/FW crash in capture and compare mode after failed sync
- Fixes for GPIB
  - Firmware crash when closing GPIB daemon, when GUI is running
  - Errors in SCPI query may hang GPIB communication
- GUI crash in "capture data" window
- N4872A: Self-test limit for VMIROUT too strict

List of known problems for 5.66 release

- See 5.63 release

Bug fixes for 5.65 release

- Improved auto calibration of temperature control circuitry (13.5G)
- Introduced new front-end hardware revision (3.3G)

List of known problems for 5.65 release

- See 5.63 release

Bug fixes for 5.64 release

- N4873A: CDR gets out of lock when system is started

List of known problems for 5.64 release

- See 5.63 release

Bug fixes for 5.63 release

- Analyzer Attenuation Correction
- Port Type Query delivers wrong result for 13G Analyzer only configurations
- Errored PRBS: check for number of possible errors strange
- Configuration Tool won't show the S/N of the clock modules
- MUI-Studio crashes on WinNT4, when saving measurement
- N4873A/75A Output Level Measurement won't stop when the full input range is used

List of known problems for 5.63 release

- File Browser - Details: Multiple instead of single selection
- Segment Editor: data window jumps back to offset 0
- Right Click shows undefined behavior
- SMSE chooses invalid block length for fast bit sync
- Installation / Deinstallation does not work any more
- XGbE Tool: CJ- and CR-Pattern on real XAUI DUT does not work
- System User Guide - Deskewing: wrong connector types of 13.5G
- Description of the Deskewing process for E4809A is incomplete.
- Setting the Delay System before establishing connection fails
- MUI: Eye Opening: ISO-BER interpolation wrong!
- GUI dies on XP OS, when screensaver is invoked
- If MUI not visible no Status events started in sync mode
- MUI always loads setting when opening a workspace or measurement
- Wrong B-1 value of concatenated scrambled multiple frames (SONET-C)
- Output Levels MUI - decimal precision of BER axis not modifiable
- Eye opening MUI - decimal precision of BER Threshold not modify
- Cable deskew not working unless common mode voltage is zeroed.
- MUI Output Timing strange Jitter Values
- Wrong tab-order in MUI Spectral Jitter / Properties

Bug fixes for 5.62 release

- MFC70.DLL incorrectly uninstalled
- Wrong Sample Threshold default vales for OLEV MUI
- GUI crashes when Data/Sequence Editor is started
- BIOS <-> MUI measurement
- Firmware -> Bios -> Eye Measurement
- Clock duty cycle calibration not properly used
- Firmware's SCPI parser gets confused by optional arguments
- Actual delay update not working reliably
- Not enough compared bits after a synchronization

List of known problems for 5.62 release

- MUI-Studio crashes on WinNT4, when saving measurement
- N4873A/75A Output Level Measurement won't stop when the full input range is used
- File Browser - Details: Multiple instead of single selection
- Segment Editor: data window jumps back to offset 0
- Right Click shows undefined behaviour
- SMSE chooses invalid block length for fast bit sync
- Installation / De-Installation does not work any more
- XGbE Tool: CJ- and CR-Pattern on real XAUI DUT does not work
- System User Guide - Deskewing: wrong connector types of 13.5G
- Description of the Deskewing process for E4809A is incomplete.
- Setting the Delay System before establishing connection fails
- MUI: Eye Opening: ISO-BER interpolation wrong!
- GUI dies on XP OS, when screensaver is invoked
- If MUI not visible no Status events started in sync mode
- MUI always loads setting when opening a workspace or measurement
- Wrong B-1 value of concatenated scrambled multiple frames (SONET-C)

Bug fixes for 5.61 release

- E4809A clock Module does not work reliably in external direct clock mode
- GUI: Help Button and F1 key broken
- New System Overview (Technical Data Sheet)
- Recall/Import of Settings created with Software Rev. 5.51, 5.52, 5.53 doesn't work for 13G systems

List of known problems for 5.61 release

- MUI-Studio crashes on WinNT4, when saving measurement
- N4873A/75A Output Level Measurement won't stop when the full input range is used

Major Enhancements in Rev. 5.6

- N4872A-75A support for MUX 32, 64, 128, 256
- N4872A-75A can be used together with E4832A and E4861B Modules

Bug fixes for 5.6 release

- N4872A/73A shown as N4874A/75A in Configuration Tool
- N4872A/73A still 74A/75A strings shown in self test messages
- Settings stored in wrong place in Windows Registry
- Module type not fully displayed for some modules
- Wrong CDR selection displayed in GUI
- Q-bus cable missing: E4805 shown in error message, even on E4809A
- Firmware crashes when a client forcefully exits
- Segment resolution mode setting only master central module
- Error Message "Not all sequencer interrupts could be handled correctly"
- GUI updating erroneous threshold value to 0
- PLL indicator sometimes red, external clock in m/s configuration
- N4873A/75A: acquire around error: min number of bits after error
- P&P: .net driver wrapping wizard generates 2 warnings
- E4809A Trigger Output (also applies for E4808A and E4805B)
- Rarely -2 is returned when using multiple commands
- N4872A/74A: SGEN:PDAT:TERM:DCON:SOUR command/query not working

List of known problems for 5.6 release

- MUI-Studio crashes on WinNT4, when saving measurement

Bug fixes for 5.53 release

- N4872A may not start if output protection is active

List of known problems for 5.53 release

- N4872A/73A shown as N4874A/75A in Configuration Tool
- N4872A/73A still 74A/75A strings shown in self test messages
- Settings stored in wrong place in Windows Registry
- Module type not fully displayed for some modules
- Wrong CDR selection displayed in GUI
- Q-bus cable missing: E4805 shown in error message, even on E4809A

Bug fixes for 5.52 release

- E4861B generator in RZ and R1 format sends 120µs pulse when stop is pressed.
- E4863B: Analyzer hangs when changing sweep delay immediately after a sync.
- N4873A: Minimal sampling time resolution not compliant to 100fs
- N4872A: Performance/Reliability issues when driving into open
- N4873A: Changing threshold produces unexpected sampling errors
- Output Amplifier Range Check – Additional check

List of known problems for 5.52 release

- N4872A/73A shown as N4874A/75A in config tool
- N4872A/73A still 74A/75A strings shown in self test messages
- Settings stored in wrong place in Windows Registry
- Module type not fully displayed for some modules
- Wrong CDR selection displayed in GUI
- Q-bus cable missing: E4805 shown in error message, even on E4809A

Bug fixes for 5.51 release

- N4873A/75A: Modification of the CDR selftest fixes occasional CDR selftest failures
- The selection of CDR is not represented in exported and saved setting file.
- E4861B: generator in RZ and R1 format sends 120µs pulse when stop is pressed.
- N4872A/73A/74A/75A: Very long time until PLL status is updated (13G/7G) (increases 1sec/ module)
- Only first clock module queried for PLL status
- Only CDR analyzer in first clock group queried for lock status
- E4805B doesn't work in master-slave configuration
- N4872A/73A/74A/75A: excessive system selftest time (3 sec. / module)
- E4808A doesn't work in master-slave configuration
- N4872A/74A cable deskew limited to 20ns, 25ns required
- E4869A/B (45G Analyzer) does no longer boot after updating to V5.50 SP x _

List of known problems for 5.51 release

- N4874A, N4875A shown as N4872A, N4873A in Config tool
- N4874A, N4875A still partly shown as N4872A, N4873A in self test error messages
- Settings stored in wrong place in Windows Registry
- Module type not fully displayed for some modules
- Wrong CDR selection displayed in GUI
- Q-bus cable missing: E4805 shown in error message, even on E4809A

Major Enhancements in Rev. 5.50 SP4

- Support of the 3.35Gbps, 7Gbps and 13.5Gbps data modules within one clock group using the 13.5Gbps Central Clock Module E4809A

Bug fixes for 5.50 SP4 release

- N4874A, N4875A deskew does not work
- N4874A, N4875A wrong header lines in self test error messages

List of known problems for 5.50 SP4 release

- N4874A, N4875A shown as N4872A, N4873A in Config tool
- N4874A, N4875A still partly shown as N4872A, N4873A in self test error messages

Bug fixes for 5.50 SP3 release

- E4811A: percentage units in optical MUI applications fails w/ error message
- E4866A, E4861B, N4872A, N4874A: Incorrect Crossover-Point setting when changing levels in disconnect mode
- Buffer overflow in compare & capture mode with captured pattern length multiple of 4 but not multiple of 8
- N4873A, N4875A Deskew does not work with Frequency Multiplier != 1
- N4872A-75A CDR improvements (self tests...)

List of Enhancements for 5.50 SP3 release

- N4872A-75A initial (limited) support for MUX 32, 64, 128, 256

List of new known problems for 5.50 SP3 release

- XGbE Tool: CRC errors shown without lane errors on XAUI port.
- XGbE Tool: CJ- and CR-Pattern on real XAUI DUT does not work.
- N4873A, N4875A N4873A/75A Fast Bit Synchronization Problems with MUX <= 128
- N4873A, N4875A captures extra bits when block length and segment resolution 32, 64, 128, 256
- N4873A, N4875A compare & acquire stop latency too large

Bug fixes for 5.50 SP2 release

- E4809A + E4866A/E4867A generates a startup errors (e.g. ERROR 21013)
- N4872A/N4874A Delay settings are not properly restored after frequency changes. This causes wrong clock out position depending on frequency history.

Bug fixes for 5.50 SP1 release

- N4872A/73A/74A/75A Delay wrong when Frequency changes
- Multiple Clients can interfere with each other.

Major Enhancements in Rev. 5.50

- Support of ParBERT 13.5Gbps Data Modules N4872A, N4873A, N4874A, N4875A and the 13.5Gbps Central Clock Module E4809A

Bug fixes for 5.50 release

- Synchronization fails when using external Start
- GUI sometimes does unnecessary stop/starts. This happened when the step size or unit of a property was changed while some properties where in error (marked red).
- MUI measurements with very big number of compared bits (e.g. 10^14) crashes for controlling modules E4861B, E4811A, E4867A
- E4863B: Self test Error in level self test when in differential mode
- E4861B & E4811A: receive memory upload doesn't work at Segment Resolution factor 4 (fatal IO error)
- E4866A: PECL 3.3V into 100Ohm (differential) predefined level doesn't work
- E4811A: Build system doesn't recognize wavelength calibration options
- VEE Pro 6.0 reports an error while parsing .fp file
- E4861B, E4811A, E4867A: If a remote program stops the machine immediately after a sync on data, sometimes a fail is reported and no bits are counted
- E4861A: cannot measure after module self test
- Memory Based Detect Segments with "0x 1" coding leak memory. Especially visible with DMUX rewiring.

Bug fixes for 5.20 SP2 release

- E4861B/E4811A: Receive Memory upload at MUX 4 doesn't work (fatal error message).
- E4811A: Build system error when calibrating for different wavelength. An E4811A that is calibrated for multiple wavelength, reports always option #000 (which is 850nm). This prevents system builder to create a system that allows use of the other wavelength.

Bug fixes for 5.20 SP1 release

- External Start Mode in Master/Slave configurations with at least one non-E4832A Data Module not working (Module Error Message: "module not in arm mode").

Major Enhancements in Rev. 5.20

- New Spectral Jitter Decomposition Tool
- Auto Sync Polarity Adjust

Spectral decomposition of jitter components with ParBERT 81250

The latest version of ParBERT 81250 software and measurement suite includes a new measurement for the spectral decomposition of jitter components. The decomposition technique allows inband- and outband-characterization of circuits and devices including PLLs and CDRs. While debugging designs, the new measurement allows the exploration of the various components of deterministic jitter.

Automatic selection of input polarity during synchronization

The synchronization is now able to find the suitable input polarity setting for the incoming signal. When enabling the automatic polarity selection, the synchronizing analyzer channel will first try to synchronize with the currently selected input polarity. If this fails, it will try to synchronize with the opposite input polarity.

Note that this feature is only available, if all analyzer channels in the system are able to select the input polarity. Currently this is only supported by E4832A (E4835A front end), E4861B (E4863B front end) and E4811A.

The input polarity after the synchronization can be queried using the input polarity commands and is displayed in the corresponding property windows.

Bug fixes for 5.20 release

None

Major Enhancements in Rev. 5.1

- New optical data analyzer module
- New tool for generating VSR4-formatted data segments
- Application manual for setting up Recirculating optical loop tests
- Special support for programming ParBERT systems via the LAN10GbE Post Processing Tool

New optical Data Analyzer Module

The new module can receive and analyze optical as well as electrical signals at data rates between 21 Mbit/s and 3.35 Gbit/s.
The E4811A data analyzer module has one channel. It includes an optical-to-electrical (O/E) converter and an electrical data analyzer. It is calibrated for 850nm wavelength.
The O/E converter includes a sensor and a comparator. External electrical components like filters can be inserted between the sensor and the comparator. The O/E converter provides a differential signal to the data analyzer.
This module makes it possible to test optical data transmitters without external O/E converters. In combination with the available E4810A data generator module, you can now test both sides of optical transceivers directly with ParBERT.
Such measurements are fully supported by the ParBERT Measurement Software.

VSR4 Frame Generator

The VSR4 Frame Generator is a tool that allows you to generate ParBERT data segments that hold test data formatted according to the implementation agreement OIF-VSR4-01.0.
The payload can be pure PRWS (pseudo random data) or data formatted as SONET frames (generated with the SONET/SDH Frame Generator).
This supports the testing of components that conform to the VSR OC-192/STM-64 interface specifications. The tool comes with online help and the manual *VSR4 Frame Generator* .

Support of Recirculating Optical Loop Tests

Recirculating loop tests are a method for simulating long-distance optical links in a laboratory. ParBERT systems can be used for performing such tests. The manual *Recirculating Optical Loop Tests* explains how optical loop tests can be set up with ParBERT.

Support for Programming ParBERT Systems via the LAN

The ParBERT software package includes libraries that provide multiple ways for users as well as for test and measurement applications to control and program ParBERT via the LAN.
The *LAN Programming Guide* provides a practical guide to programming ParBERT via the LAN using Agilent IO Libraries, Telnet, Socket connections, or all of them. The theory can be found in the manuals enclosed in the Agilent IO Libraries install package.

Bug fixes for 5.11 release

- Timing Self tests failed on 3.3G Front ends

Intermediate releases:

Bug fixes for 5.1 release

- Some 'pure prbs' polynomials not working in inverted mode
- E4810A gets into permanent error condition, when setting not plausible value

- E4810A keeps channel switched off after module self-test
- Misspelling of long form of SCPI command ...:INP:DEL:CYCLes
- SCPI programming examples not working because of blanks within the command

Major Enhancements in Rev. 5.0x

- Remote check of connector status
- The SW 5.0 supports the new 850nm 3.35Gb/s electrical-optical generator front ends E4810A (E/O Transmitter).
- RD/DJ separation:
  With the latest SW enhancement, ParBERT allows you to measure RJ, DJ and Total Jitter. The measurement method is equivalent to the BERT Scan Method (IEEE802.3ae). The ParBERT provides you a Jitter Histogram along with numerical values for the RJ, DJ, and TJ. In order to guarantee the validity of the measurement, a "quality of fit" value is also provided.
- 10GbE Post Processing Tool
- Timing Usability enhancements

New Data Generator Module

The new module can generate optical as well as electrical signals at data rates between 21 Mbit/s and 3.35 Gbit/s. With 850nm wavelength (option 001), the optical interface is in the short distance range.
The E4810A data generator module has one channel. It includes an electrical signal generator and an electrical-to-optical (E/O) converter. It features variable crossing and variable jitter. Jitter distribution can be controlled by an external voltage source.
This module can be used for stimulating optical receivers. In combination with the available electrical analyzers (like the E4863B front ends), you can stimulate optical receivers and measure the electrical response.
Such measurements are fully supported by the ParBERT Measurement Software.

10Gb Ethernet Tool

The 10Gb Ethernet Tool supports tests of 10 Gbit/s Ethernet (10GbE) transceiver devices that conform to the 10GBASE-R and XAUI specifications as defined in the IEEE 802.3 addendum for 10GbE.
Such devices are standardized and developed, for example, by the members of the Xenpak authority. The 10Gb Ethernet Tool allows you to generate ParBERT data segments holding 10GbE-formatted data as well as recommended test patterns. It enables you to execute 10GbE tests. It can automatically upload and post-process captured data.
The information on 10GbE tests has been combined in the new application manual.

Enhancements of the ParBERT User Interface

The most important enhancement refers to the frequency setup. The *segment resolution* is the length of a word in the memory of one or several ParBERT modules. Since the memory is organized to hold approximately 128k words, the word length defines the available amount of memory. Depending on the type of module and the chosen data rate, the segment resolution required for a particular port or channel can vary between one and 256 bits.
Setting the optimal segment resolution requires some insight into the way ParBERT generates bit rates
To assist users who do not wish to dig into those details, the Parameter Editor for the clock module now allows you to choose between manual and automatic mode.
In automatic mode, the program automatically calculates a suitable segment resolution.

Enhancements of the ParBERT Measurement Software

The ParBERT Measurement Software includes the DUT Output Timing/Jitter Measurement. Up till now, the jitter evaluation has only reported the total jitter (TJ).
New setup parameters and calculations have been added measurement to separate between random jitter (RJ) and deterministic jitter (DJ).

Fast Bit Synchronization

If pure PRxS data is used, Fast Bit Synchronization is a new way to synchronize analyzers to the incoming data stream. This method is fast, because it needs only few data bits and does not optimize the sampling delay. Fast Bit Synchronization does not replace the current synchronization methods. It does not report the final delay. Fast Bit Synchronization has been implemented to support first of all “Recirculating Loop Tests ”for optical fiber connections.

Remote Check of Connector Status

The front ends have built-in protection circuits, which automatically disconnect a front end if an attempt is made to operate the front end under intolerable conditions. If this happens, the user interface is neither informed nor updated. In case of a problem, it is therefore recommended to inspect the green LEDs above the front-end connectors. They indicate the physical connection status. A new command has been implemented that allows remote programs to check the connector status.

Bug fixes for 5.0 SP1 release

- E4850B + E4832A: errors when doing frequencies in the kHz range
- E4832A hangs when going from high to low frequencies w. checks switched off

Intermediate releases:

Bug fixes for 5.0 release

- 10G Ethernet Tool don’t generates 10G pattern with preamble
- Automated De-skew doesn't set the required clock multiplier/divider correctly
- Config-Tool: invisible frame entry if VXI frame numbers sequence has gaps (e.g. VXI0, VXI2 - VXI1 turned off)
- PRWS segments cannot be used with bit sync
- Wrong info updates by switching parameter editors by using the resource menu
- Standard Mode Segment Editor: Segment Padding Problem
- Changes in the SFI-5 Generator Tool: The header of SFI-5S segments will be repeated every 320 vectors. Instead Bit striping now Byte striping is used.
- E4838A self test failure in inverted mode

Major Changes in Rev. 4.5x

This revision of the Agilent 81250 software provides:
• Extended support for testing SFI-5 SERDES devices
• Support of the enhanced ParBERT 43G systems
• Support for the new N4868A 10.8 GHz booster module
• Enhancements of the ParBERT Measurement Software

Enhanced Support for Testing SFI-5 Devices

The tools for testing SFI-5 SERDES devices (SERializers/DESerializers) are the SFI-5 Frame Generator utility and the SFI-5 Post Processing Tool.
The SFI-5 Frame Generator utility is used for generating SFI-5 formatted data segments, and the SFI-5 Post Processing Tool for analyzing the captured data.
For E4861B 3.35 Gbit/s data generator/analyzer modules, a new type of data segment is provided. It specifies pure PRWS data that is formatted according to the SFI-5 standard and includes the DSC signal.
The advantage is that such a segment does not have to be generated on the ParBERT controller and downloaded—the E4861B modules generate the data by themselves, the random data as well as the Deskew channel data. This saves not only test time and data memory, but allows the use of high-order PRxS polynomials up to $2^{31}-1$.
To reflect Agilent's ongoing effort to provide not only general purpose instruments but also turnkey solutions, the information on SFI-5 has been combined in the new application manual *Testing SFI-5 Devices*.

New Module

The N4868A 10.8 GHz booster module is an add-on to the E4866A 10.8 Gbit/s data generator modules. It contains two or four signal conditioners/amplifiers for applications that require optimum signal quality.
The N4868A 10.8 GHz booster module improves the slew rates and hence reduces the transition times of the generated signals considerably.
This module can be connected between the E4866A 10.8 Gbit/s data generator module and the DUT. Its input is the differential output of one or two generator modules. You can also use the high-speed amplifiers in single-ended mode. In this mode, you can operate each amplifier separately. For example, you can connect two 10.8 Gbit/s generators—both set to single-ended operation—and amplify two separate signals.
The software supports individual parameter settings for each of the amplifiers.

New Output Level Measurement

A new measurement type has been added to the ParBERT Measurement Software. The Output Level measurement allows you to determine the bit error rate at varying receiver thresholds. This measurement can be used for investigating the behavior of the DUT. A direct result is the determination of the optimum analyzer threshold level for receiving data from the DUT with maximum confidence.

Variable Decision Threshold Method
The method used by this measurement is commonly known as *Variable Decision Threshold Method*. It provides a "vertical" analysis of the eye opening seen by the receiver(s). This method allows you to determine more than just the actual levels. The Output Level measurement calculates also the Q-factor (a measure that describes the quality of the received signal) and derived values.
These results can assist you in characterizing the device. They can also enable you to predict very low bit error rates that would take a long time to measure.

Bug fixes for 4.50 SP3 release

- E4862B Width in RZ/R1 mode not correct if Delay Control In is in use
- Information in parameter editors not correctly updated if the resource menu is invoked to change the connector

- E4838A self test failure in inverted mode
- VXI plug&play hp81200.fp function panel caused problems in .NET wrapper generator
- 10G Ethernet Tool: No Options available at the Eth. mode Square Wave Pattern
- E4862B incorrect internal termination voltage raised protection interrupt to disconnect outputs in pure differential mode
- Configuration tool crashes on particular VXI address combinations
- E4862B/E4863B Start-Stop-Stability improved, check for locked PLL
- Documentation: SAR notes added

Intermediate releases:

Bug fixes for 4.50 SP2 release

- E4869B: in CDR mode: Frequency <-> Segment-Resolution Mismatch
- Ethernet Frame Gen. Tool generates wrong 10G CRC (last) Block
- E4869B: Sampling-Phase-Adjustment Increment Limitation
- E4868B, E4869B: Overlapping Frequency Range Restriction
- E4861B: Self test/Calibration of delay circuits fails on some modules
- E4868A/B, E4869A/B: Central-Clock: Clock-Divider/Multiplier Restriction

Bug fixes for 4.50 SP1 release

- Frequency <-> Segment-Resolution Mismatch
- V4.5: Ethernet Gen. generates wrong 10G CRC (last) Block
- DMUX: Sampling-Phase-Adjustment Increment Limitation
- MUX/DMUX: Overlapping Frequency Range Restriction
- Self test/Calibration of delay circuits fails on some modules
- 40G System: Central-Clock: Clock-Divider/Multiplier Restriction

Bug fixes for 4.50 release

- Eye Opening Measurement - Reset Marker Problem. Measure an Eye Diagram (pseudo-color mode) turn on markers. Move both markers a bit, and execute "reset markers" from the context menu. This will reset the markers, however the two indicators for the lower left and upper right corners don't get reset.
- Eye Opening Measurement voltage axis labels. In eye opening measurement, sometimes the y-axis (threshold) labels get mixed up.
- Zero adjustment value is set to zero after cable Deskew
- GUI crashes when capturing data with 3.3G Modules with segment resolution 128 and using full capture memory.
- Find Pattern does not remember "Traces" or "Vectors"
- Port Editor with no connected terminals shows error message
- Segment Name Editing: Cursor Jumps to right
- No Capture Data with mix of online and offline connectors
- GUI: Port parameter editor empty predefined levels when having a mix of connected and unconnected terminals
- Incorrect period range error after import settings (when having the highest possible frequency after import there might be an out of range error because of rounding errors)
- Change frequency while system is running fails to lock CDR-PLL
- E4805B/E4808A generates "01" on ECL trigger lines on run
- Segment Import silently corrupts segment when disk is full
- Bit sync on memory based data does not work on E4861B for all MUX factors <= 32
- Deadlock on changing frequency on external clock ref source
- Switching from DMSE to SMSE causes GUI crash
- E4808A reports self test errors when using external clock mode
- Bit synchronization on memory based PRBS fails. When using maximum possible block length and doing a bit sync on memory based PRBS, then the synchronization will finish, but show a bit error rate of 0.5 afterwards.
- Rewiring Options (40G DeMUX) not accessible from SMSE

- GUI crashes on exit when two segment editors are open
- No synchronization on Memory segments with "0x1" coding. This bug was introduced in 4.3 Release
- Y2K error in File Selection dialog box

Major Changes in Rev. 4.3

This revision of the Agilent 81250 user software provides first of all enhancements and extended support of ParBERT 43G systems.

ParBERT 43G Systems with 3.35 GHz Modules

Up to now, the ParBERT 43G systems were restricted to E4861A data generator/analyzer modules, equipped with E4862A generator or E4863A analyzer front ends. From now on, ParBERT 43G systems can also be based on E4861B data generator/analyzer modules.
A ParBERT 43G pattern generator system would use eight E4861B data generator/analyzer modules with 16 E4862B generator front ends connected to the MUX module.
A ParBERT 43G error detector system would use eight E4861B data generator/analyzer modules with 16 E4863B analyzer front ends connected to the DEMUX module.

Software Enhancements

New size of the main window

When you start this revision of the ParBERT user software for the first time, you will find that the main window has been enlarged. This supports the display of the ParBERT 43G windows, especially the Connection Editor. This requires a minimum display resolution of 800 x 600 pixels.

New predefined level

A new predefined signal level has been added. It is called CML and is meant (and automatically set) for channels connected to E4868 MUX or E4869 DEMUX modules.

DEMUX rewiring

Depending on the complexity of the demultiplexer and the chosen rewiring algorithm, DEMUX rewiring can take some time. It now runs with twice the speed as before. In addition, the *Rewiring* phase is now indicated by the side of the Run/Stop buttons, like all the other phases of a test.

Bug fixes for 4.30 SP2 release

- New product overview is in the wrong branch
- SMSE causes Gui Crash

Intermediate releases:

Bug fixes for 4.30 SP1 release

- Deskew of a E4865A Analyzer Zero Adjust didn't work (Note: the MAX Multiplier is now divided by 2 [64/2= 32]

Bug fixes for 4.30 release

- E4862B: Duty Cycle distortion not available with Delay Control In
- System State inconsistent (start 2nd GUI on same running system)
- E4838: wrong voltage levels in differential termination mode
- Endless Synch on DeMUX rewiring
- Max. Frequency display of 3.3Gbit front end 3.34 instead of 3.35
- E4862A setting not recallable into E4862B system
- DeMUX-Rewiring: Worst Case Rewiring Cycles Display wrong
- E4868/69 pre-connect not performed on recall of corrupt setting
- Auto Delay Calibration fails on 40G modules
- Config Tool crashes if unknown module is in address range>128

Major Changes from Rev. 4.1 to 4.2

Revision 4.2 of the Agilent 81250 user software supports the ParBERT module and front ends for data generation and analysis at rates from 21 Mbit/s up to 3.35 Gbit/s.
In addition, the front ends E4864A and E4865A have been enhanced.

New Data Generator/Analyzer Module

The new module is:
• E4861B 3.35 Gbit/s data generator/analyzer module like the E4861A 2.7 Gbit/s data generator/analyzer module, this new module houses two front ends. Generator and analyzer front ends can be mixed.

New Data Generator/Analyzer Front ends

The new front ends that can be installed into the E4861B data generator/analyzer module are:
• E4862B 3.35 Gbit/s data generator front end
• E4863B 3.35 Gbit/s data analyzer front end
Both front ends have a maximum data memory capacity of 16 Mbit.

E4862B data generator

In addition to the extended frequency range and memory, the E4862B 3.35 Gbit/s data generator front end has features that are not available for the other generators:

• Variable signal crossing

Standard data generators produce a signal where the crossing point is at 50 % of the amplitude. For the E4862B data generator front end, the crossing point of NRZ signals can be freely adjusted between 30 % and 70 % of the signal amplitude. This allows you to generate signals with non-symmetrical eye openings.

• Voltage controlled delay

The E4862B data generator front end has an input connector. This connector allows you to connect a voltage that controls the signal delay. The linear voltage range is ±0.5 V. By varying this voltage, it is possible to generate a signal with jitter of arbitrary distribution.
Frequencies from DC to 200 MHz are supported for the delay control.

• Precision clock generation

When the E4862B data generator is connected to a pulse port, it is automatically put into clock mode, like all the generators. For this front end, you can now choose between normal and high clock performance. In high performance mode, a precision clock signal is generated, with 50 % duty cycle and very low jitter (given by the clock module—the E4808A clock module should be used).

• RZ and R1 data formats

The E4862B data generator supports not only the NRZ data format, like the E4862A data generator front end does, but also the RZ and R1 data formats.

E4863B data analyzer

The E4863B 3.35 Gbit/s data analyzer front end has a higher speed and more memory than the E4863A 2.7 Gbit/s data analyzer. Apart from this, it has the same capabilities:

- It captures and analyzes incoming data in real time
- It provides an AUX OUT connector that delivers a recovered clock
- It supports all the measurements provided by the Agilent 81250 Measurement Software

Benefits

With the new module and front ends, the Agilent 81250 Parallel Bit Error Ratio Tester addresses:

- 10 Gigabit Ethernet (10GbE) components, including 10G Ethernet
- Attachment Unit Interfaces (XAUI, 4 ┌3.125 Gbit/s) as proposed by the Xenpak Multisource Agreement
- MUX / DEMUX components (OC-48)
- Multiple electrical-to-optical (E/O) and optical-to-electrical (O/E) transceivers (VSR OC-768)
- Cross-point switching components

Enhanced Data Generator/Analyzer Front ends

An E4861A data module can accommodate the front ends E4864A and E4865A. New front ends of this type now cover a wider frequency range:
• E4864A data generator: Formerly up to 1.35 Gbit/s—now up to 1.65 Gbit/s
• E4865A data analyzer: Formerly up to 1.35 Gbit/s—now up to 1.65 Gbit/s
If new E4864A or E4865A front ends have been added to your system, it is recommended to check the front end labels that indicate the maximum frequency. The older front ends remain limited to data rates of 1.35 Gbit/s.

Software Enhancements

Analyzing a received SFI-5 pattern is not trivial. Before the bit error rate can be measured, the skew between the 16 data lines and the 17th data channel must be considered to ensure that the received PRBS data is valid.
For this purpose, the SFI5 Post Processing Tool has been developed. This tool analyzes captured SFI-5 patterns. It determines the skew and calculates the BER not only of the 16 data lines but also of the additional synchronization channel.
The SFI5 Post Processing Tool comes with its own user interface. This interface allows you to start a test, to inspect the results, and to save the captured data into a data segment.

Bug fixes for 4.20 SP3 release

E4862B: Pulse Port - Clock Mode: Delay field not updated in all conditions (Delay Control In on/off, Level Change)
E4867A: Deskew does not work in Analyzer only systems where the E4808A Trigger output must be used as reference channel
E4862B: Clock Skew inaccuracy because of internal missing update of crossing point DAC

Intermediate releases:

Bug fixes for 4.20 SP2 release

- E4862B: Duty Cycle distortion erroneously available when Delay Control In is used. Now correctly disabled in GUI.

Bug fixes for 4.20 SP1 release

- E4808A in Master / Slave configuration always shows self-test "Master Slave clock cable not connected"
- E4861B Module not mounted front-ends might generate feedbacks on the VXI bus. This for instance might cause immediate stop of the machine in capture mode.
- E4862B: Duty Cycle distortion erroneously available when Delay Control In is used. Now correctly disabled in GUI.
- E4861B some self-test messages in service mode cause the GUI to display a parser error message.

Bug fixes for 4.20 release

- SMSE: Automatic reduction of segment length reduces last vector wrong.

- Switch to SMSE when system runs causes illegal sequence manipulation.
- E4867A, E4832A, E4861A Fast Eye Mask measurement on complement input in % mode measures wrong level
- E4861A missing check for frequency multipliers < 1. Here frequency multiplier range is restricted for high segment resolution and low frequencies. E.g. Frequency 700Mhz, Segment Resolution 64 does not allow Frequency Multiplier 1/2 and 1/4, Frequency 1400Mhz, Segment Resolution 64 does not allow Frequency Multiplier 1/4.
- E4832A and E4861A: Fast Eye Mask Measurement on Complement Input with "levels in percent" fails. Workaround: specify levels in volt or use normal input.
- E4861A and E4867A: Bit-Synchronization on Memory patterns fails when using external start. This is normally not a problem because external start mode normally is not used when doing synchronization.

Major Changes from Rev. 4.0 to 4.1

Revision 4.1x of the Agilent 81250 user software supports the ParBERT 10.8 Gbit/s data generator/analyzer modules. It provides also enhancements of the Segment Editor and a new way to switch the connectors on and off.

New Data Generator/Analyzer Modules

The new modules are:

- E4866A 10.8 Gbit/s data generator module
- E4867A 10.8 Gbit/s data analyzer module

These modules are capable of creating or analyzing data streams at 9.5 Gbit/s up to 10.8 Gbit/s.
You may think of testing a multiplexer component, stimulated by four 2.7 Gbit/s generators or eight 1.35 Gbit/s generators. One single E4867A 10.8 Gbit/s analyzer can measure the serial response. Similarly, a demultiplexer can be stimulated by an E4866A 10.8 Gbit/s data generator and analyzed by four, eight, or 16 lower speed analyzers. You may also think of high-speed applications. For example, four E4866A data generator modules can be used for stimulating an OC-768 4:1 multiplexer. The serial output of this multiplexer with a data rate around 40 Gbit/s can be analyzed by a ParBERT 43G error detector system. Using a ParBERT 43G pattern generator system, you can send a serial bit stream of up to 43.2 Gbit/s to an OC-768 demultiplexer component. Using four E4867A data analyzer modules, it is now possible to analyze the parallel output of a 1:4 demultiplexer.

These high-speed modules do not have front ends. Each has one pair of differential connectors, which is identified by the software as one connector. For these modules, one channel means one module. From the user's point of view, this is the only remarkable difference to the lower speed modules. For the connection and parameter setup, the same functions of the Connection Editor and Parameter Editor are used. Automatic analyzer sampling delay adjustment and all the measurements provided by the Agilent 81250 Measurement Software can be used with the E4867A 10.8 Gbit/s data analyzer modules.

Enhancements of the Segment Editor

For testing a multiplexer, one needs parallel generated and serial expected data. Testing a demultiplexer requires serial generated and parallel expected data. The data content is the same on both sides— only the data distribution changes. To support the setup of data to be generated and expected for multiplexer and demultiplexer tests, three functions have been added to the Segment Editor, and one has been enhanced.

Deserialize function

The Deserialize function allows you to convert a serial bit stream to parallel format. This is done in the data segment. A segment holding serial data contains just one trace. With the Deserialize function, this data can be split into an arbitrary number of traces. This, for example, makes it easy to create the data expected from a demultiplexer. To adapt to the characteristics of the demultiplexer, the function provides several alternatives for sorting the data.

Serialize function

This function is the counterpart of the deserialize function. It is used to convert parallel data to serial. A segment holding multiple traces is converted to a serial segment holding one trace. Again, several alternatives are provided for sorting the data.

Find function

Formatted data is generally organized in blocks. Such blocks contain header, control, and payload data. You may wish to pursue the order of these blocks. This is supported by the Find function. This function allows you to search for a certain bit combination within a segment. You can search for parallel and serial bit patterns.

Enhanced copy and paste

When testing n:1 multiplexers or 1:n demultiplexers, you may need separate ParBERT systems on the generating and analyzing sides. This depends on the frequency ratio. Using two ParBERT systems, in turn, means using two user interfaces. You may, for example, have set up suitable test data for the generator system. But how to transfer that data to the analyzer system, so that it recognizes the expected data?
This is covered by the enhanced copy and paste functions of the Segment Editor. As soon as the Segment Editors of both user interfaces are open, you can copy and paste memory data from one to the other.

This, combined with the Deserialize/Serialize functions, makes it easy to set up all kinds of multiplexer/demultiplexer tests.

Switching Connectors ON/OFF

The tool bar of the ParBERT user interface has always had a Connectors Off/On button for disconnecting all the front ends and for re-establishing the previous connections. Switching relays in the front ends did this. For front ends with data rates above 675 Gbit/s, this behavior can be changed. It is now possible to specify whether the relays shall be switched or whether grounding shall disconnect the front ends. Especially in a production environment, grounding is a way to increase the lifetime of the ParBERT relays.

Bug fixes for 4.12 SP1 release

- List of Firmware Servers is empty
- E4869A synchronization problem with ext clk
- E4869A CDR PLL cannot lock when switching between ext and int clk

Intermediate releases:

Bug fixes for 4.12 release

- E4867A Bit synchronization for very large memory segments might hang
- E4867A Deskew sometimes does not work
- E4867A Output Timing Measurement RMS Jitter value sometimes invalid
- Firmware might hang in Pattern Find with 0K1R coding and start position is at the end of the segment
- E4832A Deskew does not work when E4866A/67A is present in same system
- Very slow bit error rate display update. Workaround was to open the Analyzer port Property Window
- E4869A could not synchronize on Memory Segments in CDR mode

Bug fixes for 4.11 release:

- Sync On Variable Mark Density PRWS crashes FW
- Gui: maximum memory segment length check
- Gui: illegal memory segments problem
- Deskew does not work when current setting uses external start
- Eye Diagram Meas - threshold checks missing
- The command <handle>:sgen:glob:per -1 results in a firmware hang up.
- MMEM:SEGM:GET? "","NON_EXISTING_SEGMENT_NAME" crashes FW
- P&P: hp81200_portHighLowLevel, hp81200_terminalHighLowLevel or hp81200_connectorHighLowLevel did not use one SCPI transaction internally
- P&P hp81200_terminalOutputTermConfig (4711, 4, DIFF) and hp81200_terminalOutputDiffImpedance (4711, 4, 100) reports an error (Martin)
- P&P hp81200_terminalOutputDiffImpedance used wrong SCPI command

Bugs introduced with SW rev. 4.0 and fixed in 4.11:

- Gui: Configuration Assert on "wrong" copied Database entry
- Config Tool: no master slave systems generated any more
- Config Tool: can't create correct 43G systems when logical addresses > 128 are used
- Detail Mode Sequence Editor - BER Threshold Edit Ctrl
- Detail Mode Sequence Editor - Edit Sync Options
- Standard Mode Sequence Editor - Rewiring triggers sequence download
- Standard Mode Sequence Editor - BER Threshold
- DeMUX Rewiring: Trace-Detection: No Rewiring with "0 x1" coded segments
- DEMO_MUX no locking of timing parameters (grey out)
- 40G Demo Settings "E4868A_DeskewCalibration" and "E4868A_PRBS_DEMO" caused errors during import

Major Changes from Rev. 3.5 to 4.0

Revision 4 supports not only all common ParBERT configurations but also the *Agilent 81250 ParBERT 43G Systems.* This is accompanied by enhancements of the Agilent 81250 Configuration Tool and the start procedure of the Agilent 81250 user software.

Agilent ParBERT 43G Systems

The Agilent 81250 ParBERT 43G is a solution for generating and analyzing electrical data streams of 38 Gbit/s up to 43.2 Gbit/s. It allows you to stimulate and analyze 16:1 multiplexers and 1:16 demultiplexers at data rates of 2.7 Gbit/s and 43.2 Gbit/s, according to the OC-768 and SFI-5 (Serdes Framer Interface 5) data range. It allows you also to determine the bit error rate of serial devices or transmission lines operated at 43.2 Gbit/s. It supports the investigation of FEC devices at 43.01841 Gbit/s including the FEC rate resulting from 255/236 overheads. The Agilent 81250 ParBERT 43G systems are offered as bundles —one for pattern generation and one for error detection. But it is also possible to upgrade existing systems. A setup for testing both multiplexers and demultiplexers would use both bundles. The bundles include also the E4808A clock module, which is superior to the well-known E4805B clock module.

Software Enhancements

An Agilent 81250 ParBERT 43G system is automatically recognized and the user software comes up with a Connection Editor, which is preconfigured.

Support of multiple user interfaces

Using both Agilent 81250 ParBERT 43G bundles means using two ParBERT user interfaces. This is required for independent clock generation and parameter setup. The capability to run more than one user interfaces has always been there. The Agilent 81250 Configuration Tool and the ParBERT user software now greatly support the use of several user interfaces:
More than one user interface can be automatically started.
Every user interface can be individually configured. The configuration parameters for each user interface include:

- Location of the firmware server (local or LAN address),
- Name of the system to be operated,
- Name of the setting to be automatically downloaded to the system.

Every user interface can easily be switched to operate one of the configured systems. Tests can be started an stopped simultaneously on two or more user interfaces and hence systems. For this purpose, the software includes the utilities “System Starter for 2 Systems ” and “System Starter for n Systems ”.

Data generation for SONET and SFI-5

The Utilities panel provides also the access to two tools used for generating data segments for the ParBERT 43G.

- The SONET SDH Frame Generator generates data that is formatted according to SONET standards (STS 3 to STS 768) or SDH (STM 1 to STM 256). This tool includes its own online help.
- The SFI5 Frame Generator generates data that is formatted according to SFI-5 standards.

External clock sources

If an external clock source is connected to the master clock module then this source determines the system clock frequency. The software now provides not only the clock multiplier but also a clock divider. This means, you can, for example, set the system clock frequency to 3/5 of the external clock frequency, or to any other arbitrary value.

PLL lock indicator

When an external clock source is used, the phase locked loop of the master clock module locks onto that source. The PLL lock indicator informs you in case the clock system could not lock or has lost its synchronization.

Automatic Rewiring of Demultiplexer Terminals

When testing demultiplexers, you apply serial data to one terminal and analyze parallel data from a number of terminals. Pure PRBS and PRWS data are generally well suited for testing demultiplexers. But if you are using memory-based data, you may encounter the problem that the data from the DUT is correct, but does not start with the first terminal —the one numbered “1 ”. This, however, is required for comparing the received data with the stored data segment. Trace 1 of the segment is expected from the first terminal, trace 2 from the next, etc.
The ParBERT now provides a means to fully automatically check the incoming data and rearrange the sequence of the terminals. As a result, the first terminal is the one that delivers the first bit of every word, the second terminal delivers the second bit, and so on, and the incoming data can be compared with the expected.

Bug fixes for 4.0 release:

- Zero Adjust in Analyzer only systems finds no signal (dependent on previous zero Adjust value)
- E4861A front ends sometimes off even if LED is on
- E4861A Cable Deskew Range Check not strict enough, Limit now 20ns
- Cross update Problem in Standard Sequence Editor
- Segment Names are not checked for valid characters
- E4805B generates error when Q-Bus cable not connected for Master/Slave configurations
- Segment import "0x1" coding erroneously accepted and treated as "0ix1"

Intermediate releases:

Rev. 3.52 SP 2

- Trigger is wrong in external start mode (E4861A)
- Second 16 bits are doubled on external start (E4861A)

Rev. 3.52 SP 1

Module Self test Errors might be shown at wrong Module (Problem introduced in 3.50 Release)

- Some small memory leaks in firmware server when closing handles (Problem introduced with 3.00 Release)
- Sweep Delay does not reflect Frequency changes

Major Changes from Rev. 3.0 to 3.5

The *Agilent 81250 ParBERT Measurement Software* now provides four measurements:

- DUT Output Timing/Jitter Measurement
- Eye Opening Measurement
- Bit Error Rate Measurement
- Fast Eye Mask Measurement

All these measurements are based on measuring the bit error rate at many points in time and many voltage levels. They are meant for characterizing data transmitting devices. An important feature of the Agilent 81250 Parallel Bit Error Tester is the automatic analyzer sampling point adjustment. This feature is used to place the initial sampling point at the optimum.

New and Enhanced Measurements

The existing measurements —DUT Output Timing/Jitter Measurement and Eye Opening Measurement —have been enhanced. New measurements have been added:

Bit Error Rate Measurement

The Bit Error Rate Measurement of the measurement software provides more and enhanced capabilities than provided by the standard user software: Stop criteria can be defined to obtain comparable results in minimum time, automatic repetition can be specified for long-term studies.

Fast Eye Mask Measurement

The Fast Eye Mask Measurement is first of all meant for production and screening tests. It is used to determine whether the eye openings of a device are within specifications. It allows obtaining pass/fail information within a few seconds.

Hardware Enhancements

Enhanced modules and front ends now provide extended frequency ranges:

- From formerly 667 MHz to now 675 MHz
- From formerly 1.33 GBit/s to now 1.35 GBit/s
- From formerly 2.67 GBit/s to now 2.7 GBit/s

These frequencies are the new G.709 and SFI5 standard data rates.
On from revision 3.5, the modules and front ends to be used with the Agilent 81250 Parallel Bit Error Ratio Tester are:

VXI modules

- E4805B, 2.7 GHz, clock module
- E4832A, 675 Gbit/s, data generator/analyzer module
- E4861A, 1.35/2.7 Gbit/s, data generator/analyzer module

Generator front ends

- E4838A, 675 Mbit/s, differential output, low voltage amplitude/offset and variable slopes generator front end
- E4843A, 675 Mbit/s, NRZ/RZ, differential generator front end
- E4864A, 1.35 Gbit/s, NRZ differential generator front end
- E4862A, 2.7 Gbit/s, NRZ differential generator front end

Analyzer front ends

- E4835A, 675 MSa/s, a pair of two differential or single-ended high sensitivity analyzer front ends
- E4865A, 1.35 GSa/s, differential input high sensitivity analyzer front end
- E4863A, 2.7 GSa/s, differential input high sensitivity analyzer front end

NOTE

The enhanced modules and front ends have the same part numbers as their predecessors. Stickers stating their maximum data rates identify them.
The extended data rates can be used on a system that comprises **only** enhanced modules and front ends. If a system includes older and newer components, for example 2.67 GHz **and** 2.7 GHz modules or front ends, then it will be still restricted to 2.67 GHz.
So, you may think of joining Agilent 's 81250 ParBERT 2.67G to 2.70G Upgrade Program and update all your older components.

Older Modules and Front ends

Important features of the Agilent 81250 Parallel Bit Error Ratio Tester are the functions for automatic analyzer sampling point adjustment and the ParBERT Measurement Software. There are older modules and front ends that do not support these features.
The following modules and front ends may be present in a system but cannot be used for typical ParBERT applications, such as measurements derived from the bit error rate or high-speed multiplexer testing:

VXI Modules

- E4805A clock module
- E4831A clock and data generator module
- E4841A data generator/analyzer module

Generator front ends

- E4842A, 330 Mbit/s, NRZ/RZ, single ended, variable transitions, 3.5 V amplitude
- E4846A, 200 Mbit/s, dual output single-ended front end

Analyzer front ends

- E4837A, 667 MSa/s, differential input high sensitivity analyzer
- E4844A, 667 MSa/s, single input front end
- E4845A, 330 MSa/s, dual input front end
- E4847A, 330 MSa/s, high-Z, dual input front end

Bug fixes for 3.52:

- Mui - DUTOutput GetTerminalCalculatedValues IsValid flag
- Mui - EyeOpening GetTerminalCalculatedValues IsValid flag
- Mui - DUTOutput clock delay tool tip always reflects absolute delay
- Mui - DUTOutput delay resolution remote command doesn't work
- Mui - EyeOpening GetMeasData returns invalid data structure
- Mui - DUTOutput GetAnalyzerSettingsName doesn't work
- Mui - EyeOpening GetAnalyzerSettingsName doesn't work
- Mui - EyeOpening delay resolution remote command doesn't work
- Mui - print does not correctly reflect pass/fail icons
- Mui - status line is not always updated
- Mui - DUTOutput calculated values invalid if phase margin <0.15ui
- Mui - DUTOutput redraw problem when running with terminals switched off
- Mui - can not load mcp files from another machine (localhost problem)
- Mui - empty window frames left in application (delete/close measurements)
- Mui - workspace browser, wrong key bindings for copy/paste in rename mode
- P&P systemSelect reports error when using a vi that was already associated with a system (now correctly switches system)
- P&P segment type change fails when having multiple segments open
- GPIB daemon locked when creating a handle on a system with no running GUI
- The GPIB demon doesn't start on a Windows 2000 system. It's not only a problem of Win2000.
  The registry entry names for the GPIB card changes again. SystemController -> SystCtrl
  and BusAddress -> BusAddr. (Back to the roots)

- CPLD programming errors not shown in default power up self test output. Workaround: switch to service mode, then the message is seen.
- Standard Mode Sequence Editor PRBS/PRWS field sometimes not correctly updated.
- 62A/64A Property Handler too course, in some situations BIOS error messages may occur
- 63A/65A unnecessary Threshold Range Check in differential mode
- E4805A Clock Multiplier does not work > 666MHz (now correct error message)
- E4835A Front end Mode not in Setting Export
- System locks up when stopping immediately after start during synchronization
- E4862A/E4864A possible error after setting import regarding parameter "width"
- Importing Segments as expression strings > 1024 Bytes length hangs the firmware
- E4838A in E4832A: Transition Times not changeable in Run Mode
- Two GUI handle conflict (_DSRA_OFF and _DSRA)
- Setting export via hp81200_settingExportToBuffer() reports error code but not error message
- If system frequency exceeds 667Mhz an error message is reported. (ExternalClockMultiplier property handler/Central A)
- Empty Front-End (within E4832A/E4841A timing parameter are not exported
- Module self test not working when having master/slave system
- E4805B (Selftest error) VCO

Intermediate release:

Rev. 3.01 SP 1

- Netmeeting crash after ParBERT installation
- E4805b Self test fails after measuring external frequency
- E4861A Fast Eye Mask fails on lower channel
- E4861A: timeouts too tight when measuring many bits
- E4861A & E4832A start/stop slower

Major Changes from Rev. 1.1x to 3.01

Revision 3.0 of the ParBERT software provides organizational enhancements as well as the new *Agilent 81250 ParBERT Measurement Software.*

Agilent 81250 Measurement Software

Revision 3.0 provides the new *Agilent 81250 ParBERT Measurement Software.* This software gives you a fast and easy-to-use access to complex bit error measurements for the Agilent 81250 Parallel Bit Error Tester (ParBERT). The following two measurement types are supported:

- DUT Output Timing/Jitter Measurement
- Eye Opening Measurement

DUT Output Timing/Jitter Measurement

The DUT Output Timing/Jitter Measurement allows measuring the time differences between the pins of a data bus. It allows also measuring the timing stability and provides a means for analyzing the jitter.

Eye Opening Measurement

The Eye Opening Measurement is used to measure the eye opening of a signal over time and voltage fully automatically and with adjustable precision. Tools are provided for comprehensive and exact analysis of the borders.

Measurement user interface

The measurement software comes with its own graphical user interface, but you can also embed the measurements into any programming environment that supports the ActiveX Component Object Model. In addition, a wrapper.dll allows including the measurements into programs written in C/C++.

Organizational Enhancements

Just a summary:
•The software installation has been completely revised.
•The ParBERT user software is no longer restricted to the Windows NT operating system but can also be installed and run under Windows 2000.
•The software now supports multiple IEEE 1394 PC-to-VXI interfaces (opt.#013). Two or more independent ParBERT systems can be controlled from one workstation.

Pseudo Random Bit Streams

The PRBS polynomials 2^9 – 1, 2^11 – 1, and 2^31 – 1 have been changed to standard polynomials

Bug fixes for 3.01

- E4805B CPLD fixes: sporadic frequency counter self test errors, sporadic sequencer memory counter self test errors
- E4832A / E4861A Synchronization on a memory based PRBS broken
- P&P could only handle 25 connections to firmware
- GPIB daemon shows assertion after fresh startup and clicking on Settings (Workaround: press ignore)
- Torx Screw driver now shipped
- Highest Frequency (e.g. 666.667 MHz @ Segment resolution 16) does not work. (Workaround 666.666MHz)
- E4805B holds ECL trigger lines High on Run
- Numerous problems when installation directory uses more than 50 characters (no problem with default path)
- Connect to server dialog endless loop when having specified an invalid IP address.
- Parameter Editor incorrectly causes implicit stop/start on close. This happens when focus was on a widget that causes stop/start

- FPGA consistency check error message after a setting load. This happens after a Deskew was done on E4832A Modules.
- Firmware server crash when using terminal index 0 for fast pass/fail queries.
- E4805B Self test errors are shown as errors instead as reports in the self test window
- P&P Help does not now about "SYNC" run state
- GPIB daemon prevents VXI access on 2-Slot Controllers
- GPIB daemon does not store its settings into registry
- Config Tool now also enables GUI startup in Controlled predefined setting

Intermediate releases:

Rev. 1.16

- E4805B sporadic frequency counter self test error

Rev. 1.15

- Version Number in _HANDLE:IDN?
- No beeping during CPLD Hardware reprogramming
- P&P import into Lab VIEW 6i documentation
- E4805B external Start not working for Segment Resolution >= 8
- Firmware Server crash during a client disconnect while the GUI queries for changes
- E4862A / E4864A output levels wrong in differential termination mode
- E4861A external start level sometimes high for a certain time before the first valid data bit comes out
- E4805B +24V Self test too strict

Rev. 1.14

- E4805B Clock Input Sensitivity (was 800mV, now 200mV)
- Fast pass/fail query erroneously returned passed for not synchronized channels
- Run state query could sometimes return wrong state at E4805B

Rev. 1.13

- E4862A 2.6666667GHz Problem (BER > 0): CPLD change and BIOS drivers, HW change

Rev. 1.12

- GPIB daemon not working on E9850A Slot Controller

Rev. 1.11

- With NI based E9850A Controllers sometimes an I/O error "unsupported bus width" occurred. As a workaround we now try several times before we give up

Major Changes from Rev. 1.08 to 1.10

In addition to the E4861A 2.67 GHz data generator/analyzer module, the Agilent 81250 system software now supports also the E4832A module.

New Module and Front end

Module E4832A

The 667 MHz data generator/analyzer module E4832A has four slots for four front ends. It can accommodate the front ends:

- E4838A, 667 Mbit/s, differential output, low voltage amplitude/offset and variable slopes generator front end
- E4843A, 667 Mbit/s, NRZ/RZ, differential generator front end
- New E4835A front end, a pair of 667 MSa/s, differential or single-ended input high sensitivity analyzer front end Compared with the E4841A data generator/analyzer module, the E4832A has twice the memory capacity and supports Compare and Capture or Compare and Acquire Around Error tests at double speed (clock rates up to 667 MHz).

It supports also the automatic analyzer sampling point adjustment.